AP-617

APPLICATION NOTE

Additional Flash Data Protection Using VPP, RP#, and WP#

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CONTENTS

PAGE

1.0 INTRODUCTION 5

2.0 FLASH DATA PROTECTION AND EXTERNAL CONTROL MECHANISMS.....5

3.0 Vpp CHARACTERISTICS.....6

3.1 V_{PP} Solution: Implementing a Lockall# Input.....7

3.1.1 5 V/12 V Lockall# DC-DC Converter Solution.....7

3.1.2 5 V Lockall# Mosfet Solution 7

3.1.3 12 V Lockall# Mosfet Solution 7

3.1.4 12 V Lockall# Mosfet with Resistor Solution.....7

4.0 P-CHANNEL ENHANCEMENT MODE MOSFET SELECTION 8

5.0 RP# AND WP# CHARACTERISTICS.....8

5.1 RP# and WP# Solutions: Implementing a Reset# and Unlock# Input.....9

5.1.1 RP# Jumper Solution.....9

6.0 INTEL® MICROCONTROLLER AND MICROPROCESSOR RESET TIMING CONSIDERATIONS 10

6.1 CPU Reset and RP# Timing.....10

6.2 CPU Reset Delay Techniques.....10

7.0 SUMMARY 11

APPENDIX A: Boot Block and FlashFile™ Memory Architecture 12

APPENDIX B: Reset Considerations 15

APPENDIX C: Potential Sources for P-Channel Mosfet Devices.....17

APPENDIX D: Additional Information.....18

PAGE

FIGURES

Figure 1. Various Levels of Protection May Be Added to Flash 14

Figure 2. When V_{PP} Resides below V_{PPLK} Program and Erase Commands to the Flash Device Are Prevented 6

Figure 3. This SmartVoltage Circuit Will Prevent Program and Erases When Lockall# Is Asserted 7

Figure 4. This Circuit Offers Reliable Lockall# Protection in a 12 V V_{PP} System.....8

Figure 5. Although This Circuit Will Cost Less to Implement, It Requires More Current Than Other Solutions 8

Figure 6. Implementing Unlock# and Reset# Inputs Using a Jumper Reduces Cost, but Also Decreases Convenience 10

Figure 7. If a Microcontroller Attempts to Fetch Code before Memory Resets, a Delay Circuit Such As This One Should Be Added 10

Figure 8. The 28F200B5-T Divides Memory into Asymmetrical Blocks and Allows the Boot Block to Be Locked.....12

Figure 9. Example Advanced/Advanced+ Boot Block Memory Top Configuration.....14

Figure 10. The 28F008S3 Has Sixteen Separately Eraseable Blocks 15

TABLES

Table 1. Control Circuit Index by Flash Density.5

Table 2. Advantages of Each V_{PP} Circuit 6

Table 3. 5 V/12 V V_{PP} Lockall# Circuit Truth Table 7

Table 4. Write Protection Truth Table for the 5 Volt Boot Block Family 9

Table 5. Write Protection Truth Table for the Advanced/Advanced+ Boot Block Flash Memory Family 9

Table 6. Reset# and Unlock# Circuit Truth Table 9

Table 7. Reset to First Data Latch 15

REVISION HISTORY

Number	Description
-001	Original Version
-002	Added data protection information for Advanced/Advanced+ Boot Block products and 3 Volt and 5 Volt FlashFile memory products. Removed information relating to discontinued products. Minor text edits.

1.0 INTRODUCTION

The introduction of reprogrammable, nonvolatile memory necessitates measures to protect stored information. Intel® Flash memory offers many advanced features to protect data integrity. Internal circuitry can help protect data at power-up, preventing spurious writes caused by power or signal glitches. Control pins, such as Reset Power-Down (RP#), Write Protect (WP#), Chip Enable (CE#), and Write Enable (WE#) inherently protect data integrity and control data flow. In today's diverse applications, system designers may desire to add optional circuitry to exploit these features. For example, general purpose I/O lines can be used to control write capability to the flash device.

This application note will first examine the functions of V_{PP}, RP#, and WP# for the boot block devices. Other devices, such as the 28F016 Intel® FlashFile™ memory, offer similar features. Several optional system-level circuit solutions which utilize V_{PP} and RP# to increase write control will then be discussed. Finally, microcontroller reset timings will be addressed. A brief discussion of boot block and FlashFile memory architectures is included in Appendix A. Table 1 provides an index of the write protection options available to each Intel Flash memory component.

Table 1. Control Circuit Index by Flash Density

Density	Available Options	Section
28F010, 28F020	V_{PP}	3.1
28F001BX, 28F002BC	V_{PP}, RP#	3.1, 5.1
28F200B5, 28F400/004B5, 28F800B5	V_{PP}, RP#, WP#	3.1, 5.1
28F008SA	V_{PP}, RP#	3.1, 5.1
28F004S3/S5, 28F008S3/S5, 28F016S3/S5, 28F160S3/S5, 28F320S3/S5	V_{PP}, RP#, and Software	3.1
28F400B3, 28F800/008B3, 28F160/016B3, 28F320/032B3	V_{PP}, RP#, WP#	3.1
28F800/008C3, 28F160/016C3, 28F320/032C3	V_{PP}, RP#, WP#, and Software	3.1

2.0 FLASH DATA PROTECTION AND EXTERNAL CONTROL MECHANISMS

Intel Flash provides several mechanisms to prevent unintentional writes. This protection is built into, and inherent to, the functions of V_{PP}, V_{CC}, RP#, WP#, and CE#. The same circuits that prevent unintentional writes make these signals well-suited for optional control circuits. In the following sections, the functions of V_{PP}, RP#, and WP# will be examined along with circuits which use these signals for greater write control.

Many systems do not need additional protection since Intel Flash inherently provides a level of protection. However, in some circumstances additional protection might be considered necessary. Unlike other types of memory, flash retains data after power has been removed. Thus, any inadvertent writes to flash are retained. Alternatively, a write to flash could place the device into a mode other than read, thus potentially preventing the system from booting properly. Flash is most vulnerable in three main circumstances:

- Unstable control signals during power-up and power-down
- During the execution of runaway code
- Control signal glitches during steady-state operation

Figure 1 shows the various levels of write protection available for use in designs.

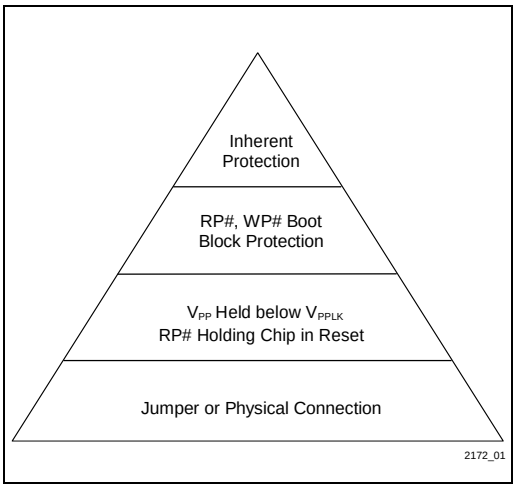

Figure 1. Various Levels of Protection May Be Added to Flash

3.0 V_{PP} CHARACTERISTICS

V_{PP} provides power to the flash device for write and erase operations and has traditionally required an external 12 V supply. Just as gasoline fuels a car engine, V_{PP} provides the gas that allows the chip to execute a write operation. Without gasoline, the car engine won't run. Similarly, without this necessary supply voltage, flash cannot write. While some Intel Flash devices provide program and erase operations at 3 V/5 V as well as 12 V, the V_{PP} pin has been retained in the pinout for the following reasons:

- Provide a means of absolute protection when grounding V_{PP}
- Maintain compliance with JEDEC dual supply standards
- Ensure easy migration for current flash-based systems
- Provide designers with maximum procurement flexibility

The dual voltage capability allows system designers to tie the V_{PP} pin to V_{CC} for single voltage designs.

The range of DC operation for V_{PP} is valid within either the write lockout range between 0 V to V_{PPLK} (V_{PPLMIN} for some devices) or the program and erase range of V_{PPHMIN} to V_{PPHMAX}, as shown in Figure 2. During a write or erase, V_{PP} must sustain at least a voltage of V_{PPHMIN}. Furthermore, the flash device locks out all write and erase operations when V_{PP} is below V_{PPLK}. Finally, write and erase operations are not guaranteed when V_{PP} is within the range of voltages between V_{PPLK} and V_{PPHMIN}.

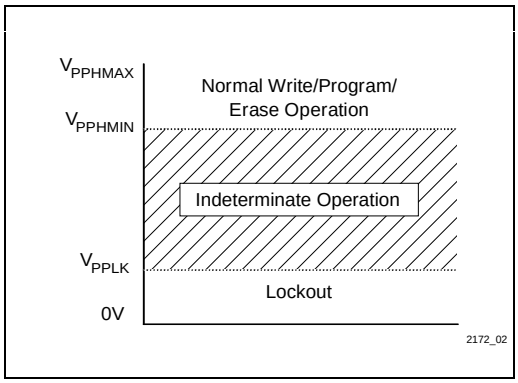

Figure 2. When V_{PP} Resides below V_{PPLK} Program and Erase Commands to the Flash Device Are Prevented

V_{PP} provides protection against spurious writes by locking out all write and erase operations when V_{PP} resides in the write lockout range between 0 V and V_{PPLK}. Any attempted writes or erases, when in this condition, will result in an error recorded in the Status Register. Read operations remain unaffected by V_{PP}.

Since V_{PP} may be tied directly to the system's voltage source, effort should be taken to ensure that the source supply voltage stays within specified tolerance levels. For most flash devices operating at 12 V, V_{PP} tolerance is ±5%.

Our 3 V and 5 V boot block products automatically sense the voltage supplied to V_{PP} during power-up or reset recovery. If the flash device senses that the source is 5 V, within the 5 V ±10% range (V_{PPH1}), on-chip charge pumps are enabled for program and erase operations. If V_{PP} is within the 12 V ±5% range (V_{PPH2}), on-chip charge pumps are disabled and the external voltage is used.

Although V_{PP} was designed to lock out writes and erases that may occur at power-up (V_{PPLK} specification), V_{PP} may also be used to add protection to a system. To implement this protection, a designer could connect a logic controlled circuit that drops V_{PP} below V_{PPLK} to prevent writes. For example, since boot code is updated infrequently in PC BIOS applications, V_{PP} may be held at ground for standard operation. Implementation of the above logic controlled circuit would allow in-system code updates, while protecting code during normal operation.

Table 2. Advantages of Each V_{PP} Circuit

Characteristic	12 V Circuit
Lowest Cost/Fewest Components	Figure 5
Least Current/Most Reliable	Figure 4

NOTES:

A DC/DC converter shutdown input may be the best solution if available.

5 V solution is reliable and requires very low operation current.

3.1 V_{PP} Solution: Implementing a Lockall# Input

As discussed, existing internal write protection circuits can be used by system designers to gain additional write control when required. A signal called Lockall#, generated by a general purpose I/O output, could prevent all write and erase commands when asserted. Several circuits designed to accomplish this are discussed below.

3.1.1 5 V/12 V LOCKALL# DC-DC CONVERTER SOLUTION

Address/data setup/hold times are dependent on when the information is latched internally. While the B3 and the LV devices both latch data on the rising edge of WE#, the B3 latches addresses on the rising edge of WE# whereas the LV latches addresses on the falling edge of WE# (see Figure 1).

Adequate address/data setup and hold timings must account for valid address/data being available at the proper edges when designing for both the LV and B3. One approach is to design the setup and hold timings such that the addresses and data are latched and held through both the rising and falling edges of WE#.

3.1.2 5 V LOCKALL# MOSFET SOLUTION

A two MOSFET configuration may be used to control the input voltage to V_{PP}, as shown in Figure 3.

The source of a p-channel, enhancement mode MOSFET is connected to the power source. The gate and drain are connected to Lockall# and V_{PP}, respectively. Operation of this circuit may be summarized as follows: a 0 V Lockall# drops V_{PP} to 0 V and a +5 V Lockall# raises V_{PP} to +5 V.

Table 3. 5 V/12 V V_{PP} Lockall# Circuit Truth Table

Lockall#	Q1	Q2	Q3	V_{PP}
Low	Off	On	Off	0 V
High	On	Off	On	~V_{SOURCE}

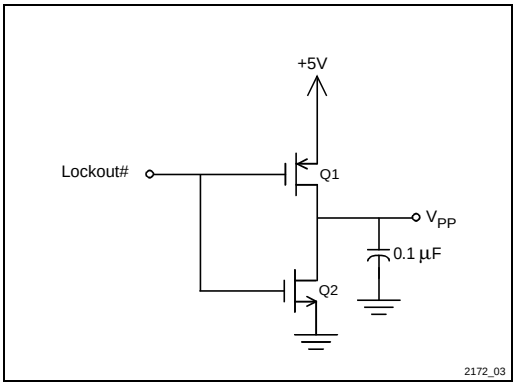

Figure 3. This SmartVoltage Circuit Will Prevent Program and Erases When Lockall# Is Asserted

3.1.3 12 V LOCKALL# MOSFET SOLUTION

Another method of implementing a Lockall# control is shown in Figure 4. A p-channel enhancement mode MOSFET, Q1, is used to transfer 12 V from its source to its drain, V_{PP}. When Lockall# is asserted, Q3 turns on causing a current across R1. The resulting voltage drop at the gate of Q1 causes Q1 to turn on, delivering 12 V to V_{PP}, minus a small voltage drop across Q1. Table 3 shows the truth table of operation.

3.1.4 12 V LOCKALL# MOSFET WITH RESISTOR SOLUTION

The cost of the circuit, discussed in Section 3.1.3, may be reduced by removing the inverter and replacing one of the n-channel MOSFETs with a resistor as shown in Figure 5. The resistor, R2, will increase the amount of current drawn through Q1. To calculate this additional current use Ohm's Law. If V_{PP} equals 12.0 V, then:

$$12.0\ V = i \times 10\ K\Omega$$

Solving for i yields 1.2 mA. Ensure that the power source can meet the maximum current demand of flash plus the current through the resistor.

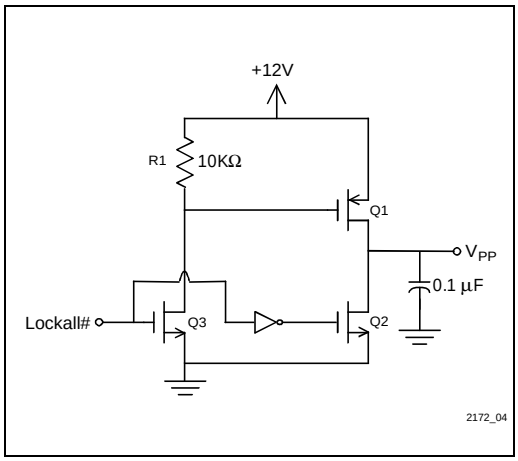

Figure 4. This Circuit Offers Reliable Lockall# Protection in a 12 V V_{PP} System

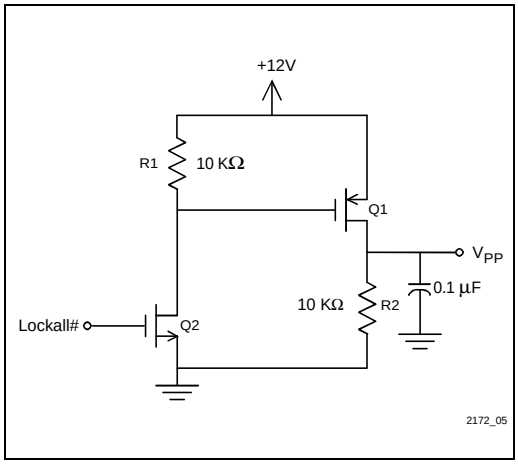

Figure 5. Although This Circuit Will Cost Less to Implement, It Requires More Current Than Other Solutions

4.0 P-CHANNEL ENHANCEMENT MODE MOSFET SELECTION

Selection of the P-Channel MOSFET is critical to proper operation. If a different device is used, ensure that V_{PP} tolerances and other specifications are met.

Two main characteristics must be taken into account when choosing the p-channel enhancement mode MOSFET: price and performance. Since V_{PP} must not drop below 11.4 V for 12 V V_{PP}, or 4.5 V for 5 V V_{PP}, the transistor must guarantee a relatively low V_{DS} voltage drop when on. Because the price of the transistor may be directly related to this voltage drop, specified by the resistance r_{DS}, choose the largest r_{DS} allowable within the power supply tolerance.

For example, if a 12 V flash device obtains power from a DC-DC converter with a 3% output tolerance, the maximum voltage drop across the transistor should be no more than 0.24 V. This may be calculated by taking 3% of 12 V, then subtracting the result from the maximum allowable voltage drop of 5% of 12 V, or 0.6 V.

$$12\ V \times 5\% = 0.6\ V$$
$$12\ V \times 3\% = 0.36\ V$$
$$0.6\ V - 0.36\ V = 0.24\ V$$

r_{DS} may now be calculated using Ohm's Law. Assuming a maximum current of 30 mA during a write cycle, $r_{DS} = 8\Omega$.

$$0.24\ V = 30\ mA \times r_{DS}$$

Thus a device with r_{DS} less than 8Ω should be selected.

NOTE:

All currents specified in the Intel Flash memory datasheets are in RMS unless otherwise noted.

5.0 RP# AND WP# CHARACTERISTICS

RP# controls three different functions: reset, deep power-down, and boot block unlocking. When RP# equals V_{IL}, the device is in reset and deep power-down mode. In this mode, the device's outputs are in a high impedance state, the Write State Machine is reset, and the device draws minimum current. Furthermore, all write and erase commands are ignored, providing another means of data protection during power-up and power-down. The device requires a minimum access time t_{PHQV} to access valid data. For a more complete discussion of reset timing, flash t_{PHQV} times, and Intel® microcontroller reset timings, refer to Section 6.0 and Appendix B.

During normal read/write operation RP# will be set to V_{IH}. At this voltage, the boot block, in Intel® Boot Block products, remains locked to writes and erases. However, all commands to other blocks return valid results. For Intel FlashFile memory products, all blocks are unlocked to writes.

For Intel Boot Block flash products, when RP# equals V_{HH}, the boot block becomes unlocked and may be written to or erased. This state overrides any control from the WP# input.

The WP# control pin, locks and unlocks the boot block, on boot block products, much like RP#. Since many applications will not have access to a 12 V source, WP# provides control of boot block locking and unlocking with a logic-level signal.

The state of WP# is only relevant when RP# equals V_{IH}. When WP# equals V_{IH}, the boot block is unlocked. Deasserting WP# to V_{IL} locks the boot block. However, on the 5 Volt Boot Block, when RP# equals V_{HH}, the boot block will unlock, regardless of the assertion level of WP#. Refer to Table 5 for a complete truth table of WP# and RP#. Refer to Table 5 for a complete truth table for Intel® Advanced/Advanced+ Boot Block devices.

5.1 RP# and WP# Solutions: Implementing a Reset# and Unlock# Input

In some applications, the system design may require the functionality of both a lock and reset signal. For 28FxxxB5/B3 products, reset and lock inputs can be tied directly to RP# and WP# respectively. However, for flash products without WP#, optional circuits may be needed. Several circuits, which provide this level of control, will be discussed in the following sections.

The operation of this circuit is summarized in Table 7.

5.1.1 RP# JUMPER SOLUTION

For applications with infrequent boot code updates, a jumper circuit is an option. This solution greatly reduces the cost of implementation, but also reduces the convenience of in-system updating. An example jumper configuration may be seen in Figure 7. In this configuration, the jumper connects RP# to the reset signal during normal operation and is switched to pull RP# up to 12 V when the boot block needs to be reprogrammed.

Table 4. Write Protection Truth Table for the 5 Volt Boot Block Family

Write Protection Provided	Operating Mode	V_{PP}	RP#	WP#
Lock All Blocks	Read Only	V_{IL}	X	X
Reset/All Blocks Locked	Reset/Deep Power-Down	$\geq V_{PPLK}$	V_{IL}	X
Unlock All Blocks	Standard Operation	$\geq V_{PPLK}$	V_{HH}	X
Lock Boot Block	Standard Operation	$\geq V_{PPLK}$	V_{IH}	V_{IL}
Unlock All Blocks	Standard Operation	$\geq V_{PPLK}$	V_{IH}	V_{IH}

Table 5. Write Protection Truth Table for the Advanced/Advanced+ Boot Block Flash Memory Family

V_{PP}	WP#	RP#	Write Protection Provided
X	X	V_{IL}	All Blocks Locked
V_{IL}	X	V_{IH}	All Blocks Locked
$\geq V_{PPLK}$	V_{IL}	V_{IH}	Lockable Blocks Locked
$\geq V_{PPLK}$	V_{IH}	V_{IH}	All Blocks Unlocked

Table 6. Reset# and Unlock# Circuit Truth Table

Reset#	Unlock#	Q1	Q2	RP#	WP#
Low	Low	Off	Off	0 V	0 V
Low	High	Off	Off	0 V	0 V
High	Low	On	On	~V_{PP}	5 V
High	High	Off	Off	5 V	0 V

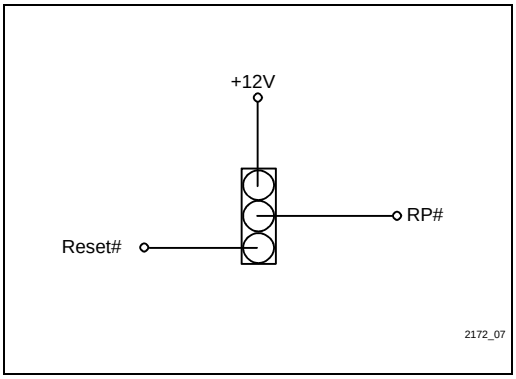

Figure 6. Implementing Unlock# and Reset# Inputs Using a Jumper Reduces Cost, but Also Decreases Convenience

6.0 INTEL® MICROCONTROLLER AND MICROPROCESSOR RESET TIMING CONSIDERATIONS

Every processor family available has a unique reset process and requires a different amount of time to execute the first instruction fetch. When interfacing memory to a processor, several factors should be examined.

One such consideration which must be addressed is the location of boot code, since loading the boot code is generally part of the reset process. If the processor does not have internal memory, it must access the boot code through an external memory bus. Thus, the memory devices must have already returned from the reset state by the time the CPU fetches data from the memory bus. In many systems, RP# and the CPU's RESET# are tied together. If the memory unit becomes available after the controller expects data, a solution must be devised to hold the CPU's request for data until memory is fully reset.

6.1 CPU Reset and RP# Timing

For flash applications, the processor's reset line may be tied to RP#. Thus, the system and CPU are in reset when RP# is at V_{IL}. To determine if the flash device will return from reset in time to meet the processor's request for boot code, the t_{PHQV} specification must be examined. Since t_{PHQV} includes flash access time, the processor may latch data off the memory bus after this time has elapsed.

To illustrate reset timings, consider a 25 MHz 80C196NP, which may execute its first instruction fetch as early as 120 ns after reset. Since t_{PHQV} for the 28F800B5-70 is specified at 450 ns, a RESET# delay would be required. However, no delay would be required for a 33 MHz Intel386™ embedded processor since the first instruction fetch would occur 510 ns after reset.

Table 7, in Appendix B, lists the specifications for the deassertion of reset to data valid for several Intel microprocessors and microcontrollers.

6.2 CPU Reset Delay Techniques

Because some CPUs return from reset faster than memory, a method must be employed to delay the processor reset. To prevent the processor from fetching erroneous data, an RC network may be inserted between the reset line and the reset pin of the processor. One such circuit is shown in Figure 8.

The Reset Source input could represent a number of signals. For example, a PowerGood signal or user-initiated reset may be connected to this input. The resistor and capacitor should be chosen to create a long enough delay to ensure flash resets. To ensure a rapid trigger from the reset voltage to normal operating voltage, a Schmitt-Trigger should be used, keeping in mind the assertion level of the processor's Reset# input. Finally, a diode in parallel with the resistor allows a quick discharge of CPU Reset# when switching from a voltage high to voltage low.

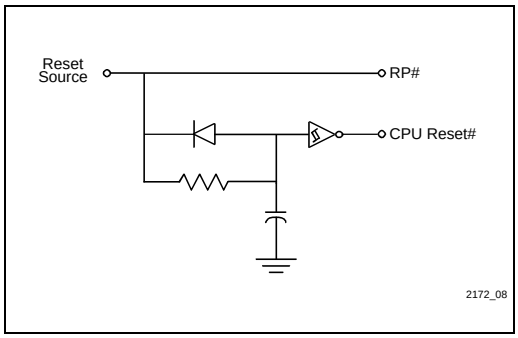

Figure 7. If a Microcontroller Attempts to Fetch Code before Memory Resets, a Delay Circuit Such As This One Should Be Added

To calculate the resistor and capacitor values, use the equation:

$$V_C(t) = V_S + (V_0 - V_S)e^{-t/RC}$$

For example, if an Intel® 80C196NP microcontroller running at 25 MHz interfaces with a 28F400B5, a minimum delay of 180 ns must be inserted to ensure valid data upon reset or power-up. If the Schmitt-Trigger switches voltage, from logic low to logic high, at V_{T+} = 0.6 V and the source voltage V_S = 5 V then the equation becomes:

$$0.6\ V = 5\ V - 5Ve^{-180/RC}$$

Solving for RC yields 1.41×10^{-6}. The resistance and capacitance may then be chosen accordingly. Since this equation yields the minimum RC requirement, this value may be adjusted for guardband.

7.0 SUMMARY

The various control and power inputs of Intel Flash memory are highly versatile. These control signals have circuitry on-chip which prevent unintentional writes to the device and may also be used for additional levels of protection. Several optional circuits were presented in this application note which would give the system design an additional level of protection against unwanted writes.

APPENDIX A
BOOT BLOCK AND FlashFile™ MEMORY ARCHITECTURE

Intel Flash offers two blocking architectures to address the needs of today's applications. FlashFile memory architecture divides memory into 64-KB blocks, while the Boot Block memory architecture divides memory asymmetrically into differing sized blocks and allows one of these blocks to be locked. This lockable block, called the boot block, can only be written when specific control pins are asserted.

Boot Block Architecture

The Boot Block flash architecture was designed for applications which require in-system updates, but have critical code which must be protected. For example, PC BIOS may require in-system updates, however, the boot code requires additional protection since the system cannot boot-up if this code becomes corrupted.

5 Volt Boot Block

Intel offers Boot Block architectures with the boot block on the bottom or at the top of the memory array. The 28F200B5-T is an example of the top architecture. Memory is divided into five blocks with the 16-KB boot block residing at the top of the memory array. Next, two 8-KB parameter blocks, a 96-KB main block, and a 128-KB main block follow (see Figure 8).

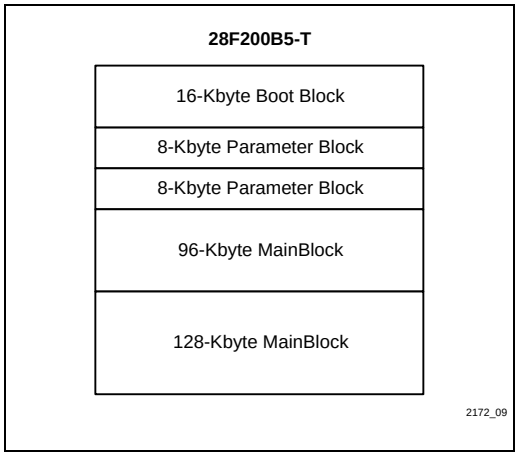

Figure 8. The 28F200B5-T Divides Memory into Asymmetrical Blocks and Allows the Boot Block to Be Locked

Advanced/Advanced+ Boot Block Architecture

For lower voltage applications, Intel also offers the Advanced/Advanced+ Boot Block architecture with the boot block on the bottom or at the top of the memory array. The 28F800B3-T is an example of the top architecture. Memory is divided into eight 8-KB parameter blocks, followed by 64-KB main blocks. Driving WP# to V_{IL} locks the upper two parameter blocks in the top configuration (lower two parameter blocks in the bottom configuration). See Figure 9.

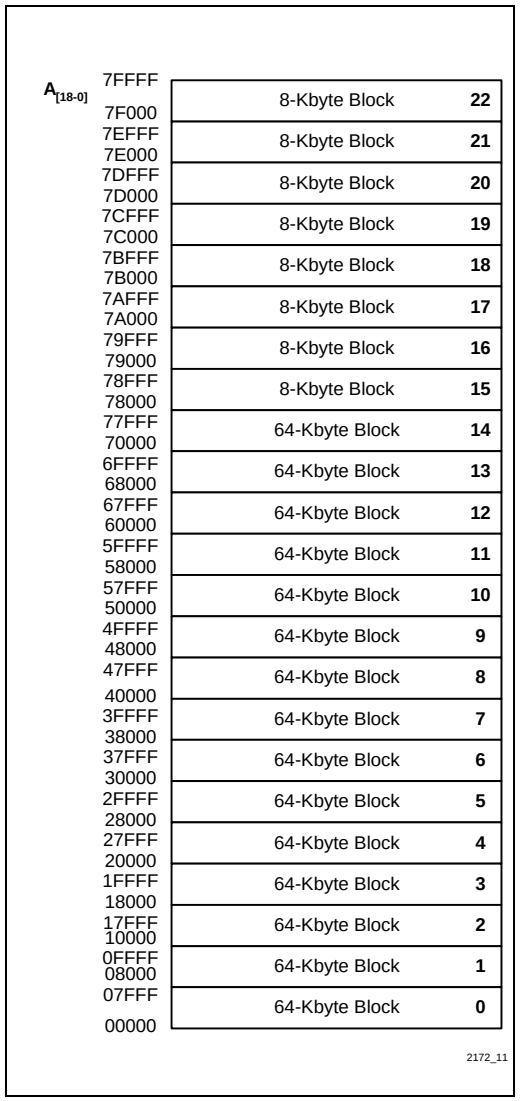

Figure 9. Example Advanced/Advanced+ Boot Block Memory Top Configuration

FlashFile™ Memory Architecture

Other applications require a more symmetric approach to memory. The FlashFile memory architecture organizes the memory array into equally sized blocks. For example, the 28F008SA, shown in Figure 10, has sixteen separately erasable 64-KB blocks. This architecture allows disk emulation as well as in-system updateability for embedded applications.

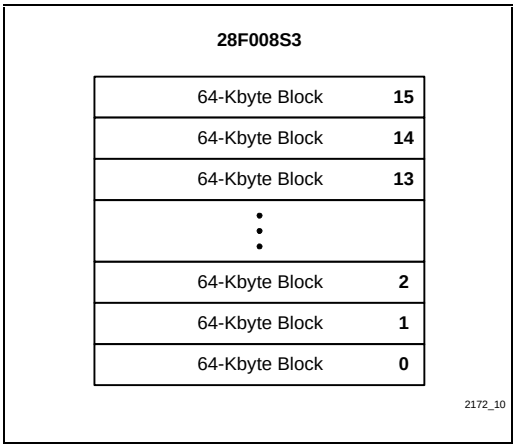

Figure 10. The 28F008S3 Has Sixteen Separately Eraseable Blocks

APPENDIX B
RESET CONSIDERATIONS

Table 7. Reset to First Data Latch

	No. of CLK Cycles	12 MHz (ns)	16 MHz (ns)	20 MHz (ns)	24 MHz (ns)	25 MHz (ns)	33 MHz (ns)	40 MHz (ns)	50 MHz (ns)	66 MHz (ns)
i486™ SX Intel® DX2™ Processor	217						6510		4340	3255
i386™ EX Processor	350		21875	17500		14000	10500			
80186	14	1167		700		560		350		
i960® Processor	32		2013	1600		1280	960			
MCS® 96 Controller	3	249	189	150		120				
MCS® 251 Controller	34	2833	2125							
MCS® 51 Controller	24	2000	1500	1200	1000					

NOTES:

Timings provided for all available speeds at time of publication (no speeds in shaded areas).

Specifications are provided for comparison only. Consult datasheets for current timing specifications.

APPENDIX C
POTENTIAL SOURCES FOR P-CHANNEL MOSFET DEVICES

Toshiba Semiconductor

Toshiba offers one of the smallest surface mount MOSFETs available. The 2-3F1F package occupies a space of 2.5 mm x 2.9 mm and is ideal for mobile applications. Toshiba also offers a JEDEC standard TO-220 through-hole package.

United States:

9775 Toledo Way
Irvine, California 92718
Tel: (714) 455-2000
Fax: (714) 859-3963

Europe:

Hansallee 181
D-40549
Düsseldorf, Germany
Tel: 0211-52960
Fax: 0211-5296400

Asia:

10F Lippo Sun Plaza
28 Canton Road
Tsim Sha Tsui
Kowloon, Hong Kong
Tel: 37 56 111
Fax: 37 50 969

Harris Semiconductor

Harris offers many low r_{DS}, p-channel power MOSFETs. The RFD10P03L is a competitively-priced power MOSFET that is available in both a through-hole and surface mount package.

United States:

1301 Woody Burke Road
Melbourne, Florida 32901
Tel: (407) 724-7000

Europe:

Mercure Center
100 Rue de la Fusee
1130 Brussels, Belgium
Tel: 32 2 246 21 11
Fax: 32 2 246 22 05/ ...09

Asia:

Shinjuku NS Bldg. Box 6153
2-4-1 Nishi-Shinjuku
Shinjuku-Ku, Tokyo 163-08 Japan
Tel: (81) 03-3345-8911
Fax: (81) 03-3345-8910

Siliconix (TEMIC)

Siliconix offers one of the lowest r_{DS} logic level PFETs available. The S08 package is part of the “Little Foot” series and is an 8-pin surface mount package.

United States:

2201 Laurelwood Road
P.O. Box 54951
Santa Clara, CA 95056-9951
Tel: (408) 988-8000
Fax: (408) 727-5414

Europe:

TEMIC Telefunken
Microelectonic GmbH
Theresienstrasse2
74072 Heilbronn, Germany
Tel: 49 7131 67-0
Fax: 49 7131 67-2340

Asia:

TEMIC Microsystems Hong Kong, Ltd.
Suite 1701 World Finance Center
South Tower, Harbour City
17 Canton Road, Tsishatsui
Kowloon, Hong Kong
Tel: 852 23 789 789
Fax: 852 23 755 733

Silconix, cont.

TEMIC (S) Pte. Ltd.
AEG Building #02-00
25 Tampines Street 92
Singapore 1853
Republic of Singapore
Tel: 65 788 6668
Fax: 65 788 3383

Micrel Incorporated

Micrel offers both a small package and low-cost p-channel enhancement MOSFET. The SOT-143 package is a 4-terminal surface mount device.

Micrel, Inc.
1849 Fortune Drive
San Jose, CA 95131
Tel: (408) 944-0800
Fax: (408) 944-0970

NOTE:

This list is intended for reference only and in no way represents all companies that produce p-channel enhancement mode MOSFETs. Since this industry develops many new products each year, Intel recommends that the designer contact the vendors for the latest products. Intel Corporation assumes no responsibilities for circuitry other than circuitry embodied in Intel products. No other circuit patent licenses are implied.

APPENDIX D
ADDITIONAL INFORMATION(1,2)

Order Number	Document
290645	*3 Volt Advanced+ Boot Block Flash Memory; 28F800C3, 28F160C3, 28F320C3*
290599	*5 Volt Boot Block Flash Memory; 28F200B5, 28F004/400B5, 28F800B5*
290598	*3 Volt FlashFile™ Memory; 28F004S3, 28F008S3, 28F016S3*
290580	*3 Volt Advanced Boot Block Flash Memory; 28F004/400B3, 28F008/800B3, 28F016/160B3, 28F320B3*
290406	*5 Volt Boot Block Flash Memory 28F001BX*
292215	*AP-657 Designing with the Advanced+ Boot Block Flash Memory Architecture*

NOTE:

1. Please call the Intel Literature Center at (800) 548-4725 to request Intel documentation. International customers should contact their local Intel or distribution sales office.
2. Visit Intel's World Wide Web home page at http://www.Intel.com for technical documentation and tools.